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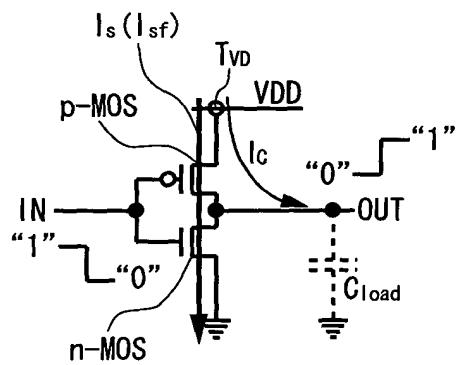
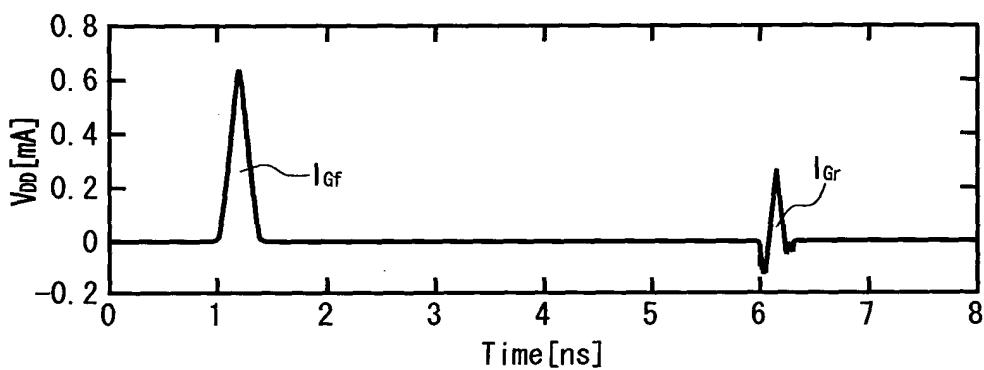
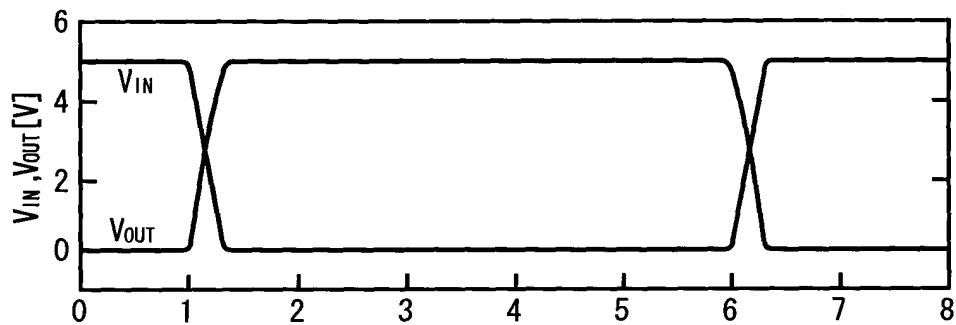


FIG. 1C

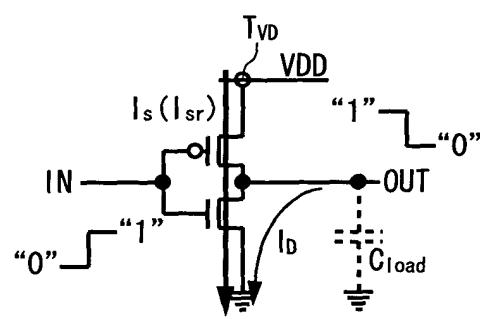


FIG. 1D

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FIG. 2A

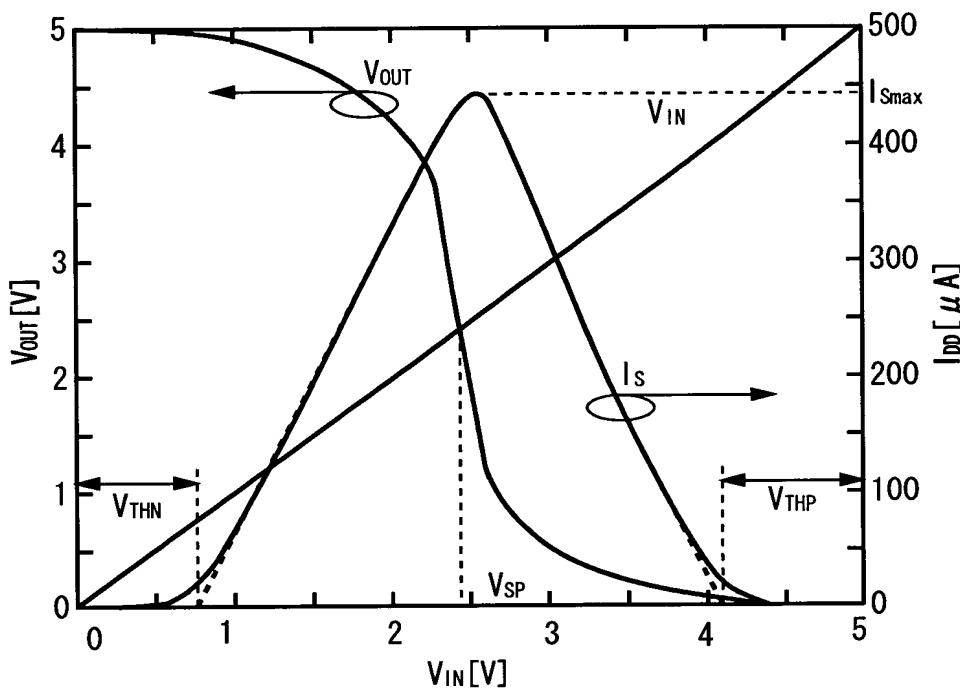
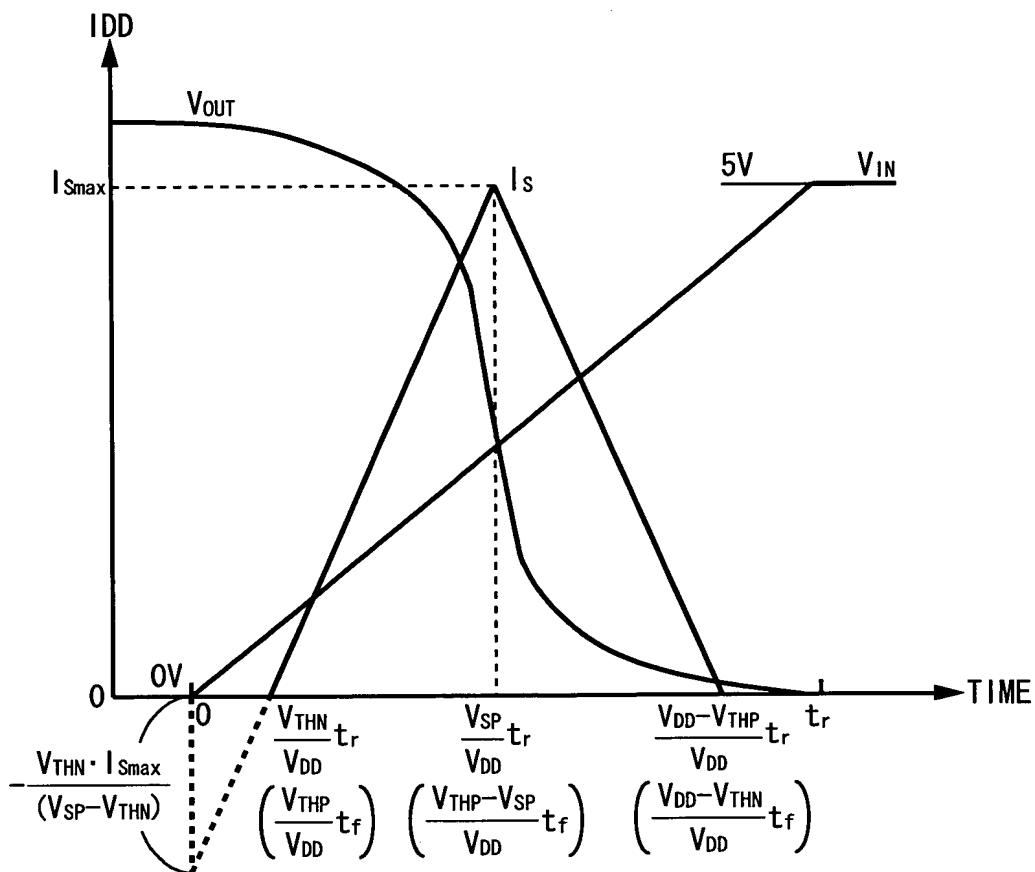


FIG. 2B



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FIG. 3A

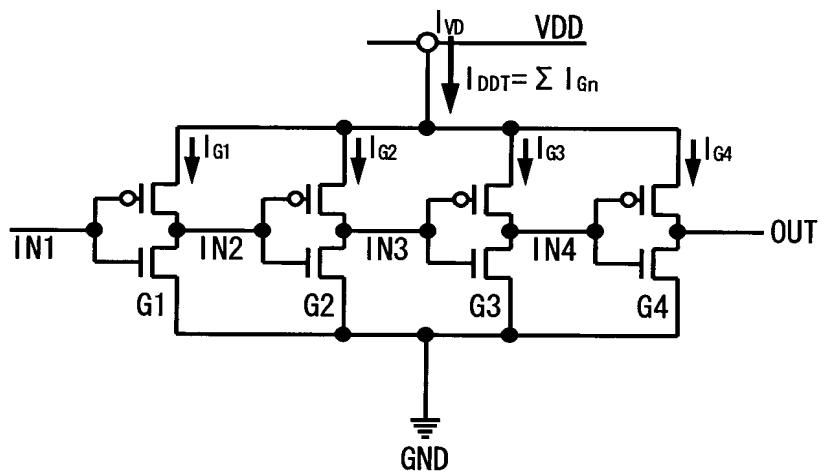


FIG. 3B

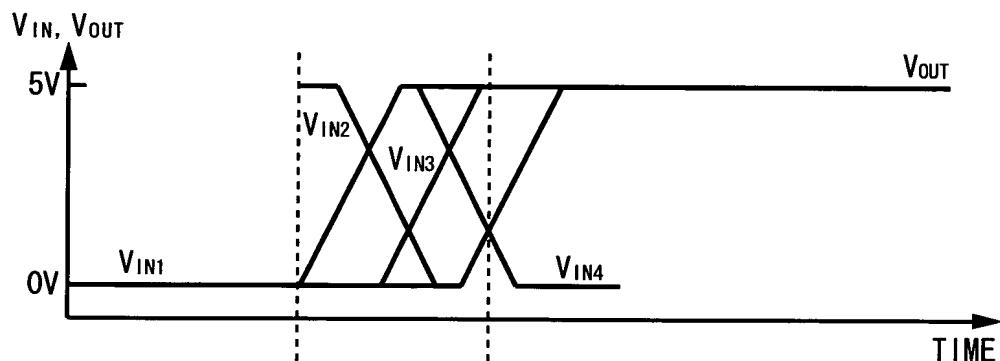
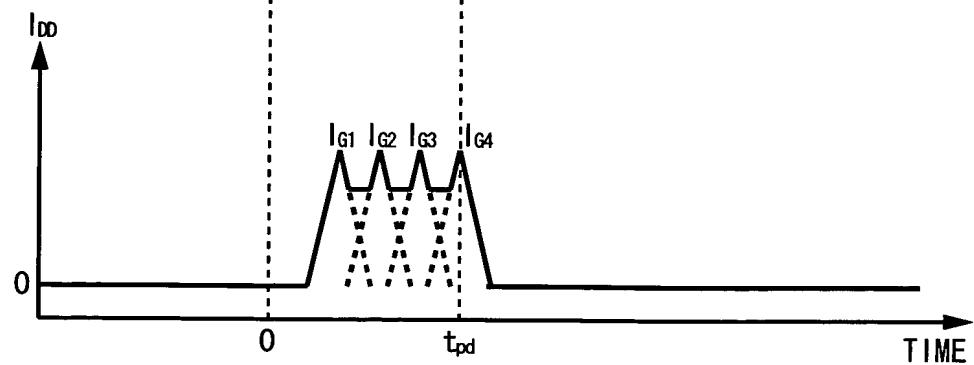


FIG. 3C



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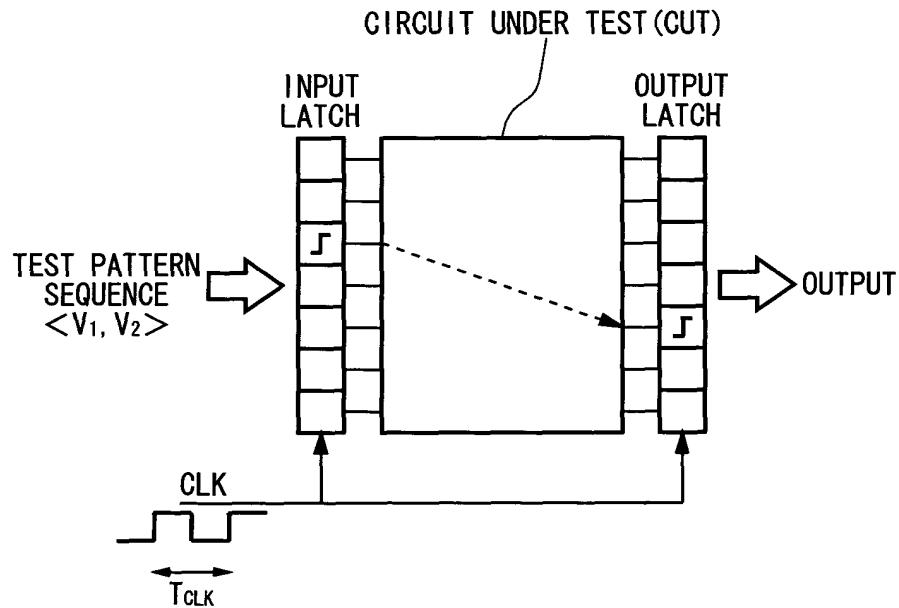


FIG. 4A

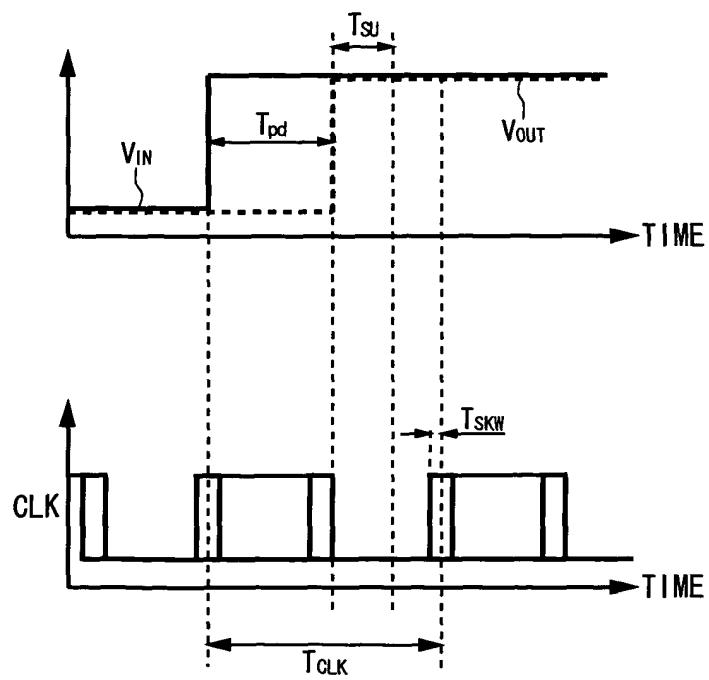
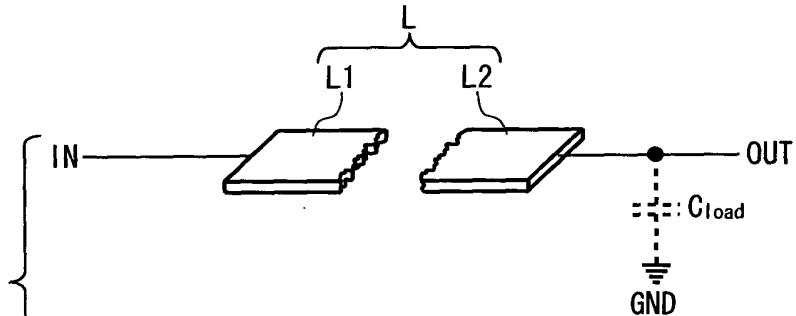
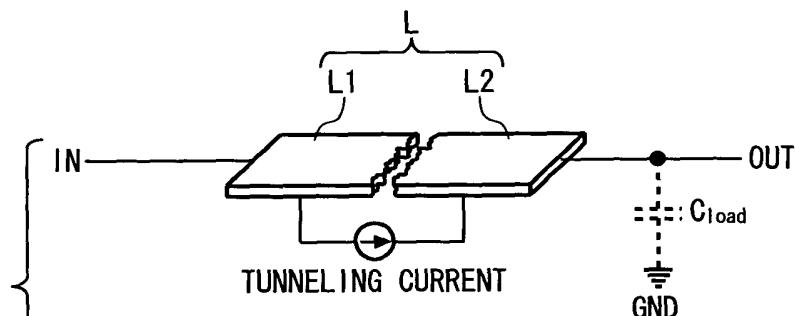


FIG. 4B

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**FIG. 5A****FIG. 5B****FIG. 5C****FIG. 5D**

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FIG. 6A

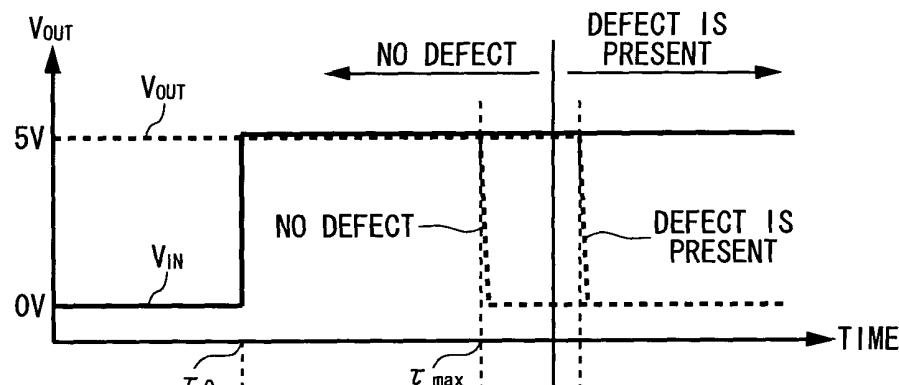
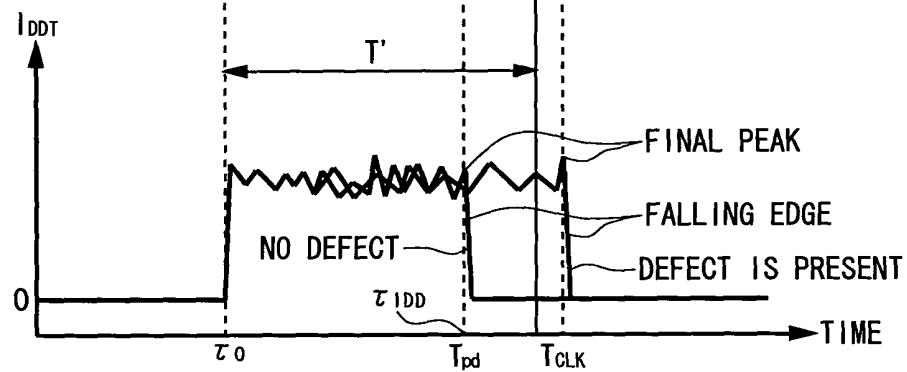


FIG. 6B



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FIG. 7A

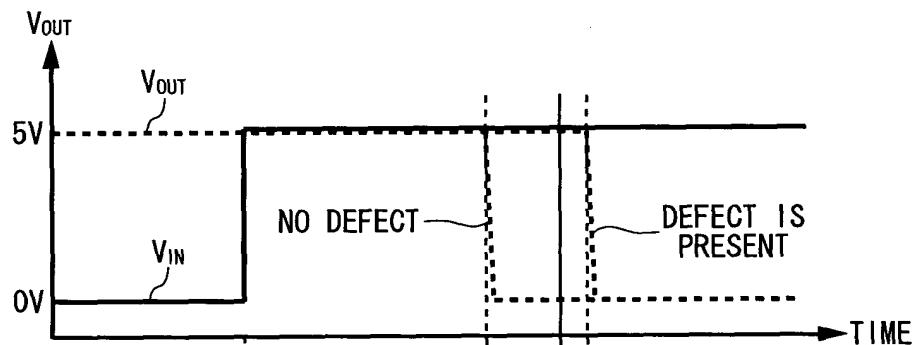
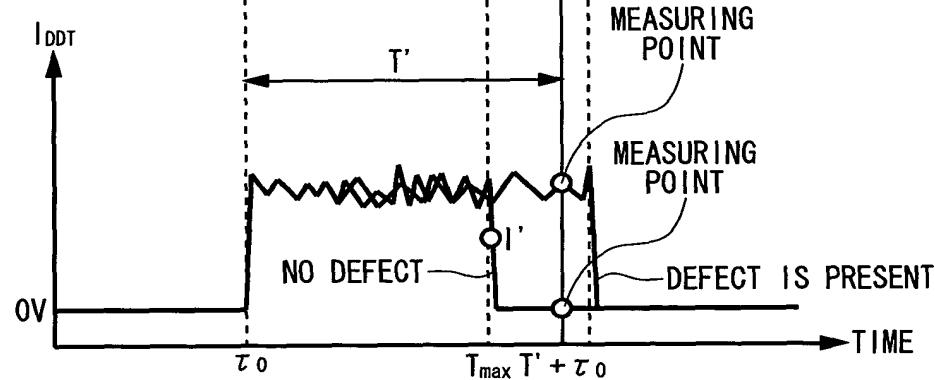


FIG. 7B

NO DEFECT:  $i_{DDT}(T' + \tau_0) \leq I'$ DEFECT IS PRESENT:  $i_{DDT}(T' + \tau_0) > I'$

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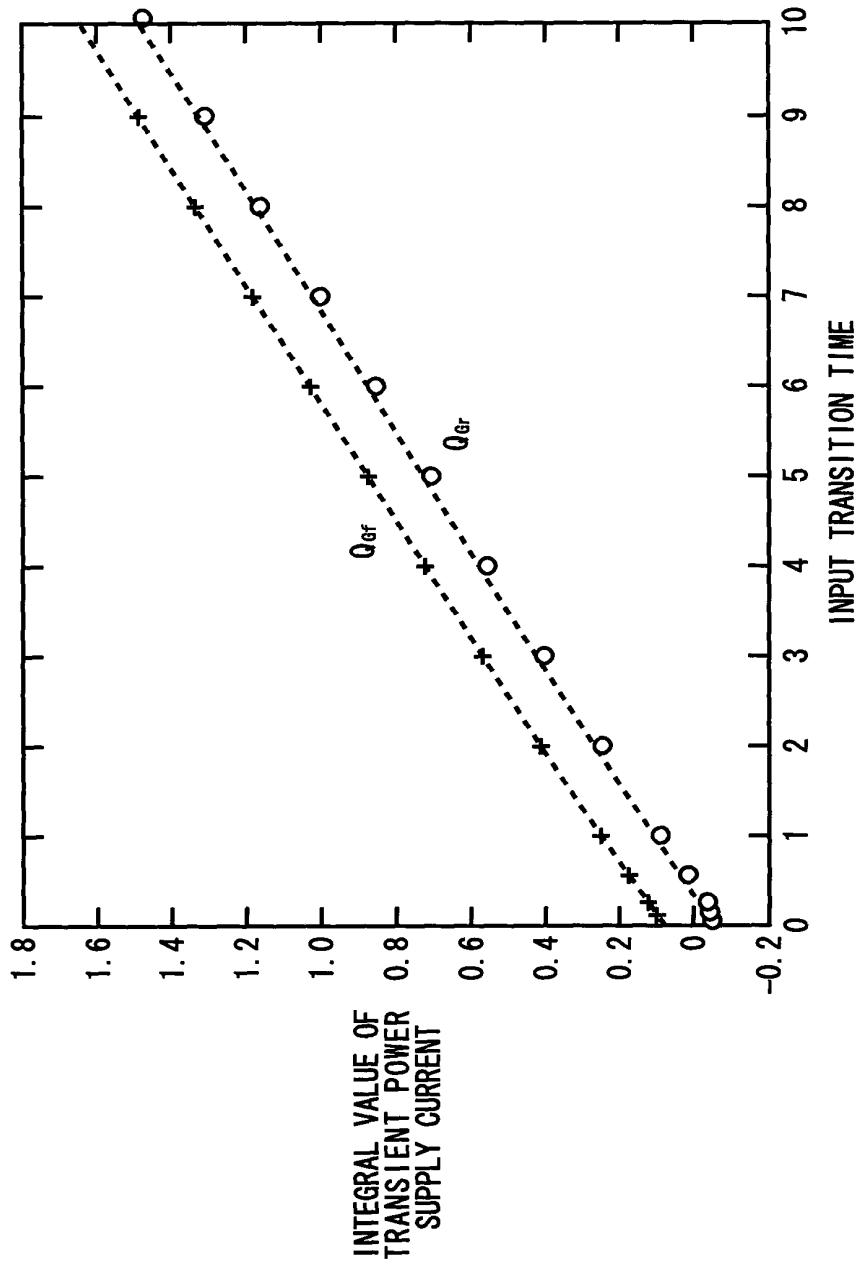


FIG. 8

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FIG. 9A

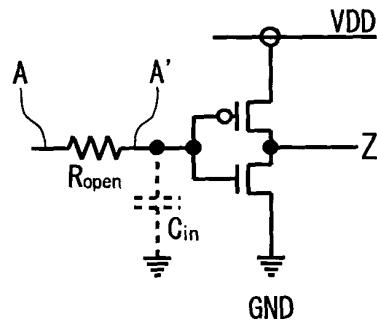


FIG. 9B

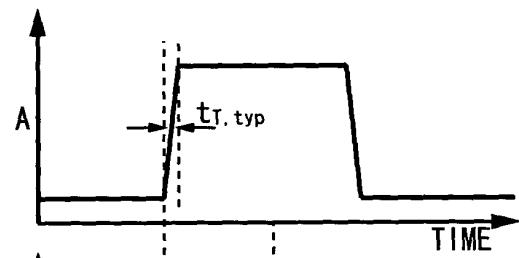
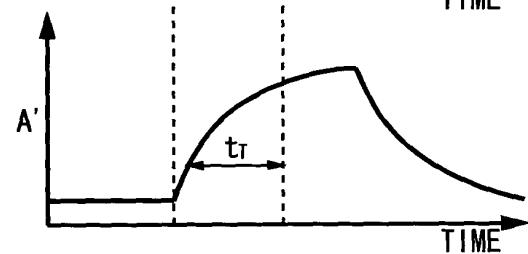


FIG. 9C



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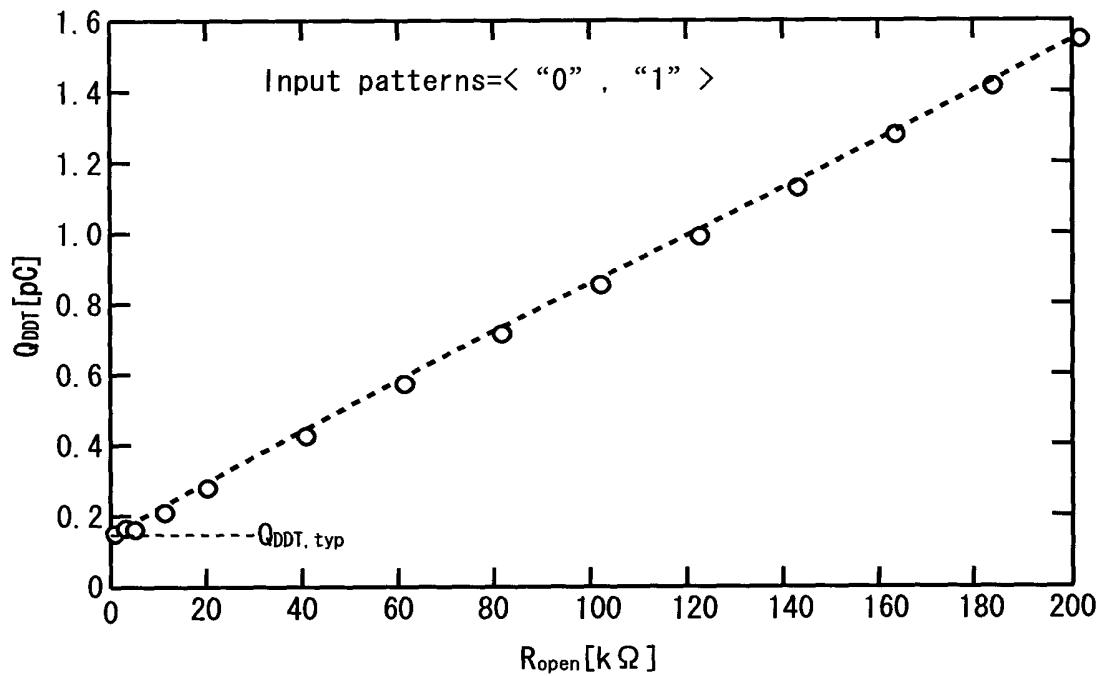


FIG. 10

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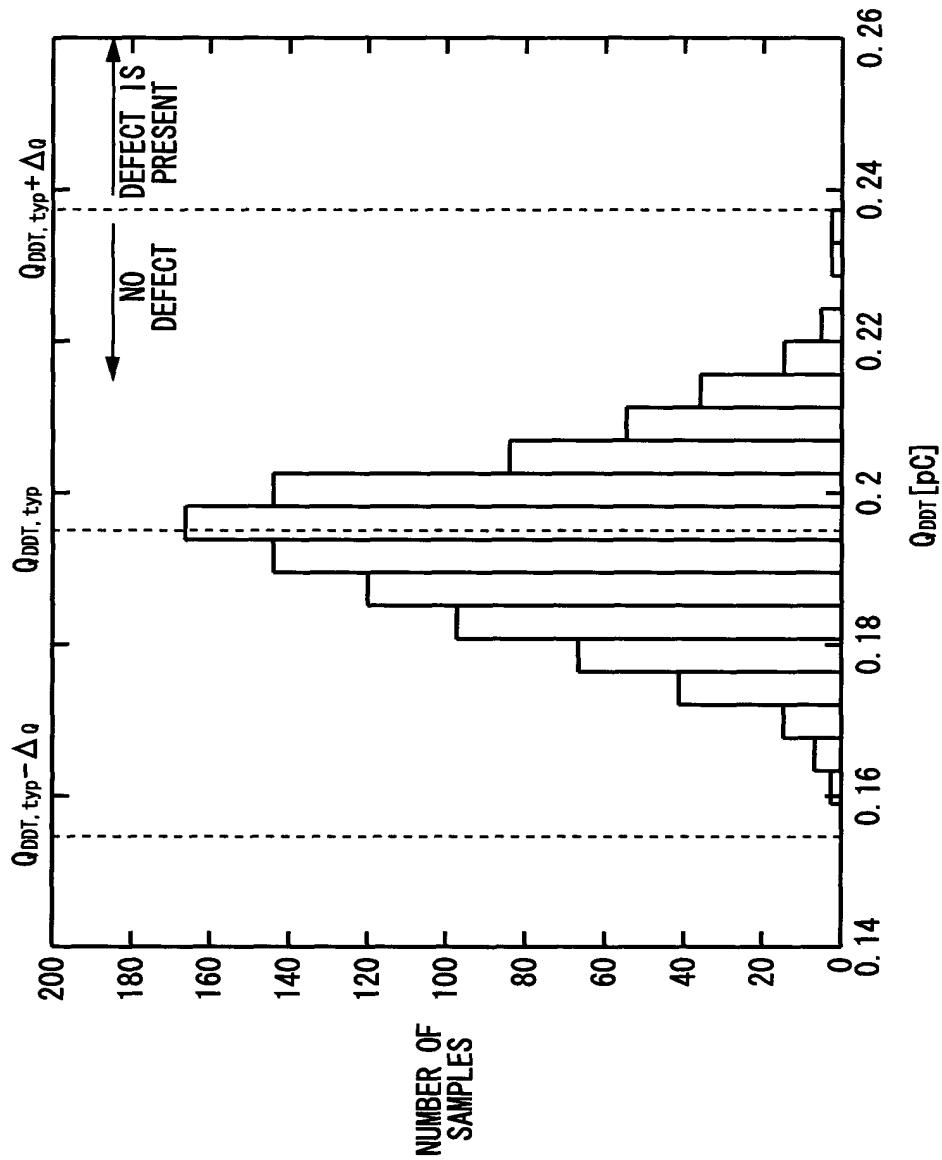


FIG. 11

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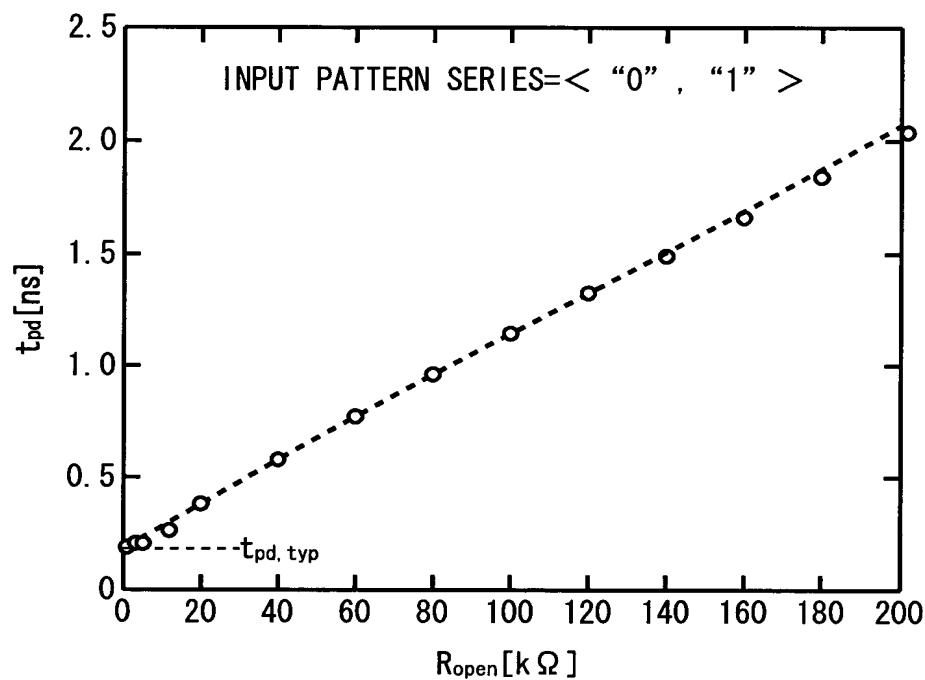


FIG. 12

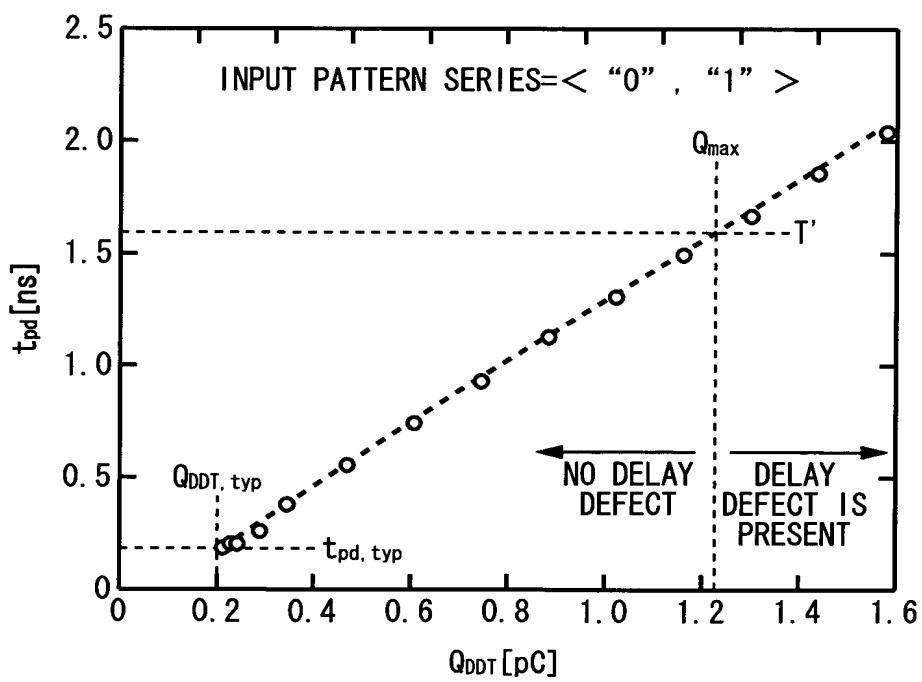


FIG. 13

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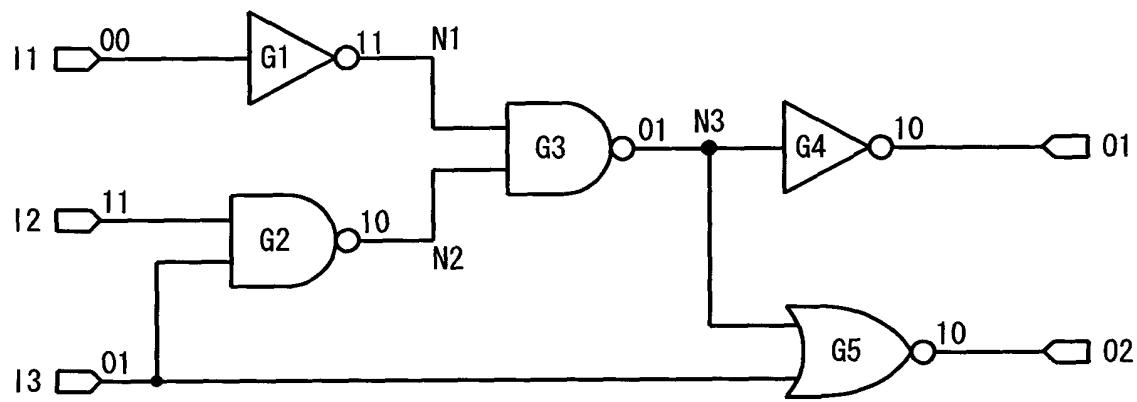


FIG. 14

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TEST PATTERN SEQUENCE ID NO.	INPUT TERMINAL			INTERNAL NODE			OUTPUT TERMINAL		DETECTABLE FAULTY GATE
	I1	I2	I3	N1	N2	N3	O1	O2	
T1	0	0	R	1	1	0	1	F	G5
T2	0	1	R	1	F	R	F	F	G2, G3, G4, G5
T3	1	0	R	0	1	1	0	0	—
T4	1	1	R	0	F	1	0	0	G2
T5	0	R	0	1	1	0	1	1	—
T6	0	R	1	1	F	R	F	0	G2, G3, G4
T7	1	R	0	0	1	1	0	0	—
T8	1	R	1	0	F	1	0	0	G2
T9	R	0	0	F	1	R	F	F	G1, G3, G4, G5
T10	R	0	1	F	1	R	F	0	G1, G3, G4
T11	R	1	0	F	1	R	F	F	G1, G3, G4, G5
T12	R	1	1	F	0	1	0	0	G1
:	:	:	:	:	:	:	:	:	:

FIG. 15

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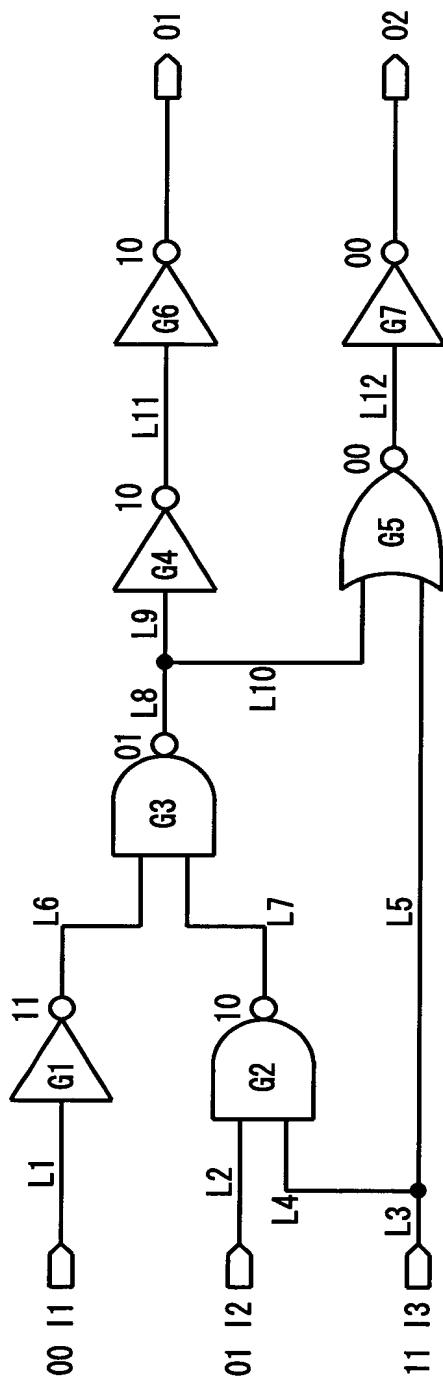


FIG. 16

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TEST PATTERN SEQUENCE ID NO.	INTERNAL SIGNAL LINE												OUTPUT TERMINAL 01	DETECTABLE DEFECTIVE INTERNAL SIGNAL LINE 02
	INPUT TERMINAL	1	2	3	4	5	6	7	8	9	10	11	12	
T1	0	0	R	0	0	R	R	1	1	1	1	F	1	L3, L5, L12
T2	0	1	R	0	1	R	R	1	F	F	F	F	F	L3, L4, L5, L7, L8, L9, L10, L11, L12
T3	1	0	R	1	0	R	R	0	1	0	0	0	0	—
T4	1	1	R	1	1	R	R	0	F	0	0	0	0	L3, L4
T5	0	R	0	0	R	0	0	0	1	1	1	1	1	—
T6	0	R	1	0	R	1	1	1	F	F	F	0	F	L2, L7, L8, L9, L11
T7	1	R	0	1	R	0	0	0	1	0	0	0	0	—
T8	1	R	1	1	R	1	1	0	F	0	0	0	0	L2
T9	R	0	0	R	0	0	0	F	1	F	F	F	F	L1, L6, L8, L9, L10, L11, L12
T10	R	0	1	R	0	1	1	F	1	F	F	0	F	L1, L6, L8, L9, L11
T11	R	1	0	R	1	0	0	0	F	1	F	F	F	L1, L6, L8, L9, L10, L11, L12
T12	R	1	1	R	1	1	1	F	0	0	0	0	0	L1
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:

FIG. 17

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TEST PATTERN SEQUENCE ID NO.	INPUT SIGNAL			INTERNAL NODE			OUTPUT TERMINAL		DETECTABLE FAULTY PATH
	I1	I2	I3	N1	N2	N3	O1	O2	
T1	0	0	R	1	1	0	1	F	<I3, O2>
T2	0	1	R	1	F	R	F	F	<I3, N2, N3, O1> <I3, N2, N3, O2>
T3	1	0	R	0	1	1	0	0	—
T4	0	1	R	0	F	1	0	0	—
T5	0	R	0	1	1	0	1	1	—
T6	0	R	1	1	F	R	F	0	<I2, N2, N3, O1>
T7	1	R	0	0	1	1	0	0	—
T8	1	R	1	0	F	1	0	0	—
T9	R	0	0	F	1	R	F	F	<I1, N1, N3, O1> <I1, N1, N3, O2>
T10	R	0	1	F	1	R	F	0	<I1, N1, N3, O1>
T11	R	1	0	F	1	R	F	F	<I1, N1, N3, O1> <I1, N1, N3, O2>
T12	R	1	1	F	0	1	0	0	—
:	:	:	:	:	:	:	:	:	:

FIG. 18

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TEST PATTERN SEQUENCE ID NO.	INPUT TERMINAL		INTERNAL SIGNAL LINE						OUTPUT TERMINAL		DETECTABLE FAULTY PATH		
	I1	I2	I3	I4	I5	I6	I7	I8	I9	I10	I11	I12	I1
T1	0	0	R	0	0	R	R	1	1	1	1	F	<I3, I3, I5, I12, 02>
T2	0	1	R	0	1	R	R	1	F	F	F	F	<I3, I3, I4, I7, I8, I9, I11, 01>
T3	1	0	R	1	0	R	R	0	1	0	0	0	<I3, I4, I7, I8, I10, I12, 01>
T4	1	1	R	1	1	R	R	0	F	0	0	0	<I3, I3, I4, I7, I8, I10, 01>
T5	0	R	0	0	R	0	0	0	1	1	1	1	<I3, I3, I4, I7, I8, I10, 01>
T6	0	R	1	0	R	1	1	1	F	F	F	F	<I2, I2, I7, I8, I9, I11, 01>
T7	1	R	0	1	R	0	0	0	1	0	0	0	<I2, I2, I7, I8, I9, I11, 01>
T8	1	R	1	1	R	1	1	0	F	0	0	0	<I1, I1, I6, I8, I10, I12, 02>
T9	R	0	0	R	0	0	0	F	1	F	F	F	<I1, I1, I6, I8, I9, I11, 01>
T10	R	0	1	R	0	1	1	F	1	F	F	F	<I1, I1, I6, I8, I9, I11, 01>
T11	R	1	0	R	1	0	0	0	F	1	F	F	<I1, I1, I6, I8, I9, I11, 01>
T12	R	1	1	R	1	1	1	F	0	0	0	0	<I1, I1, I6, I8, I10, I12, 02>
:	:	:	:	:	:	:	:	:	:	:	:	:	:

FIG. 19

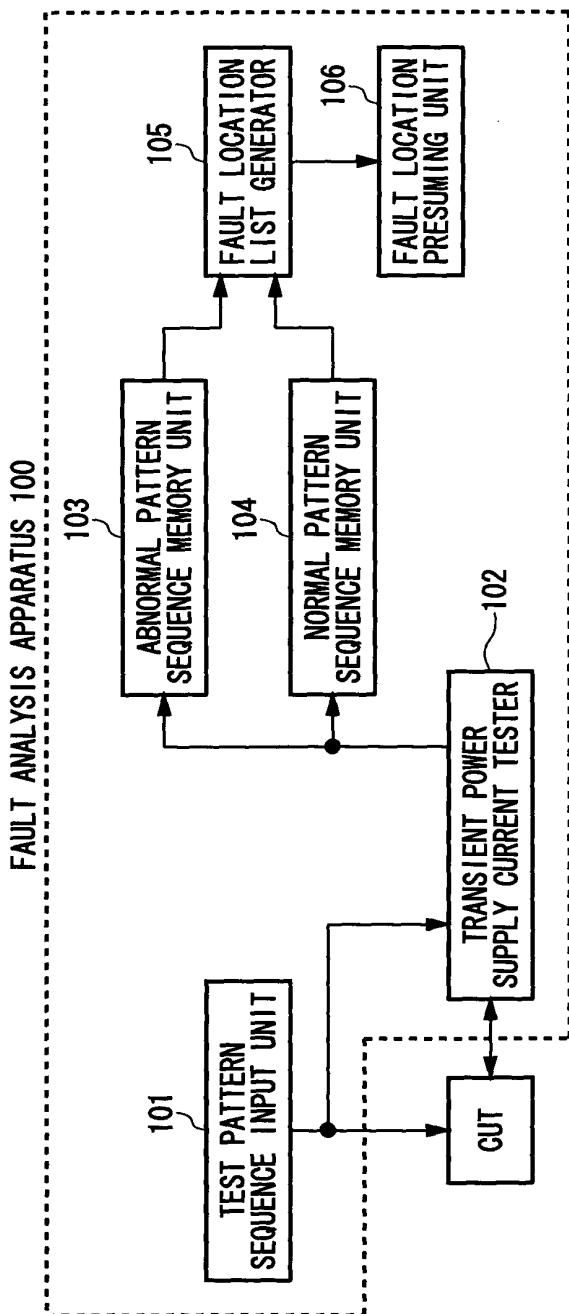


FIG. 20

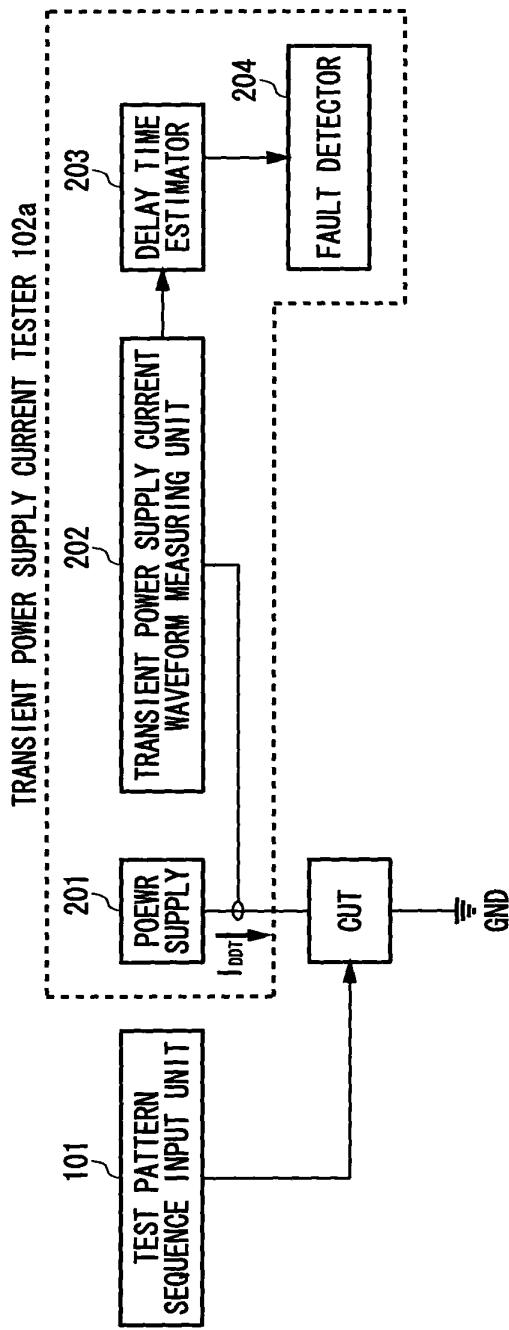


FIG. 21

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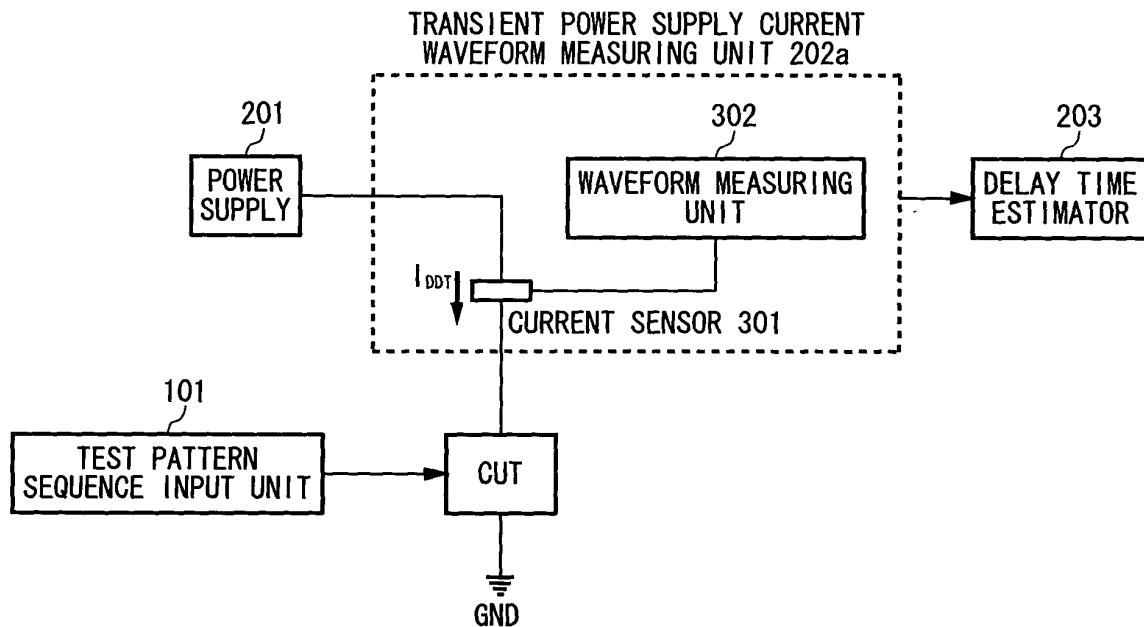


FIG. 22

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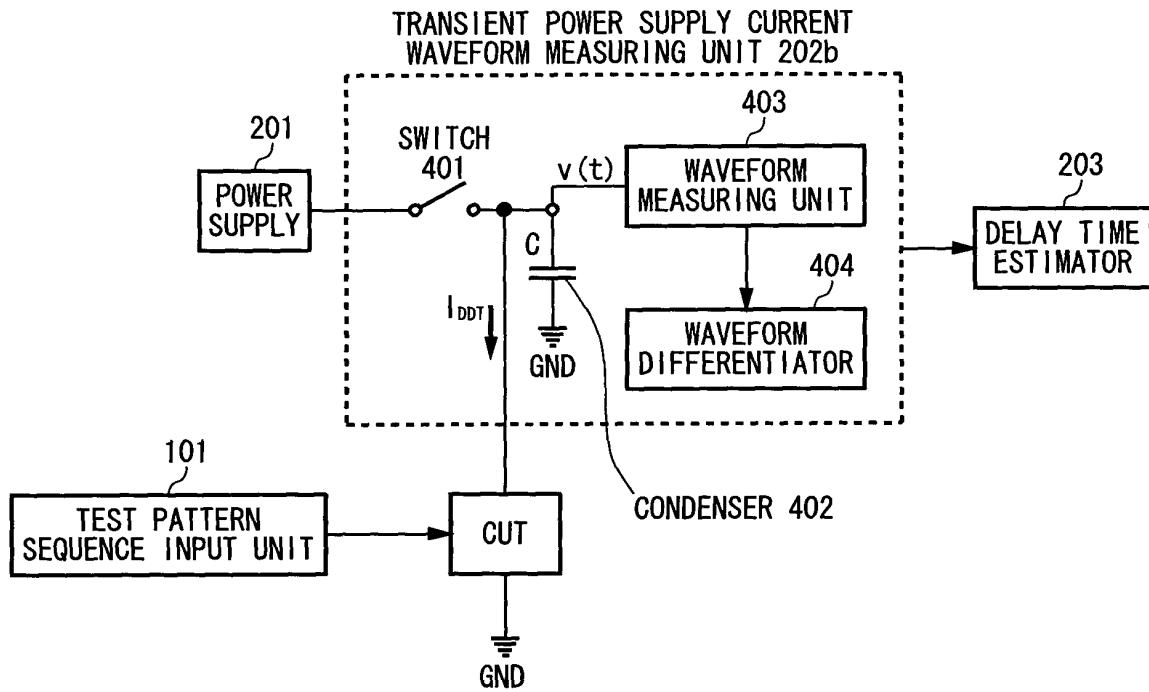


FIG. 23

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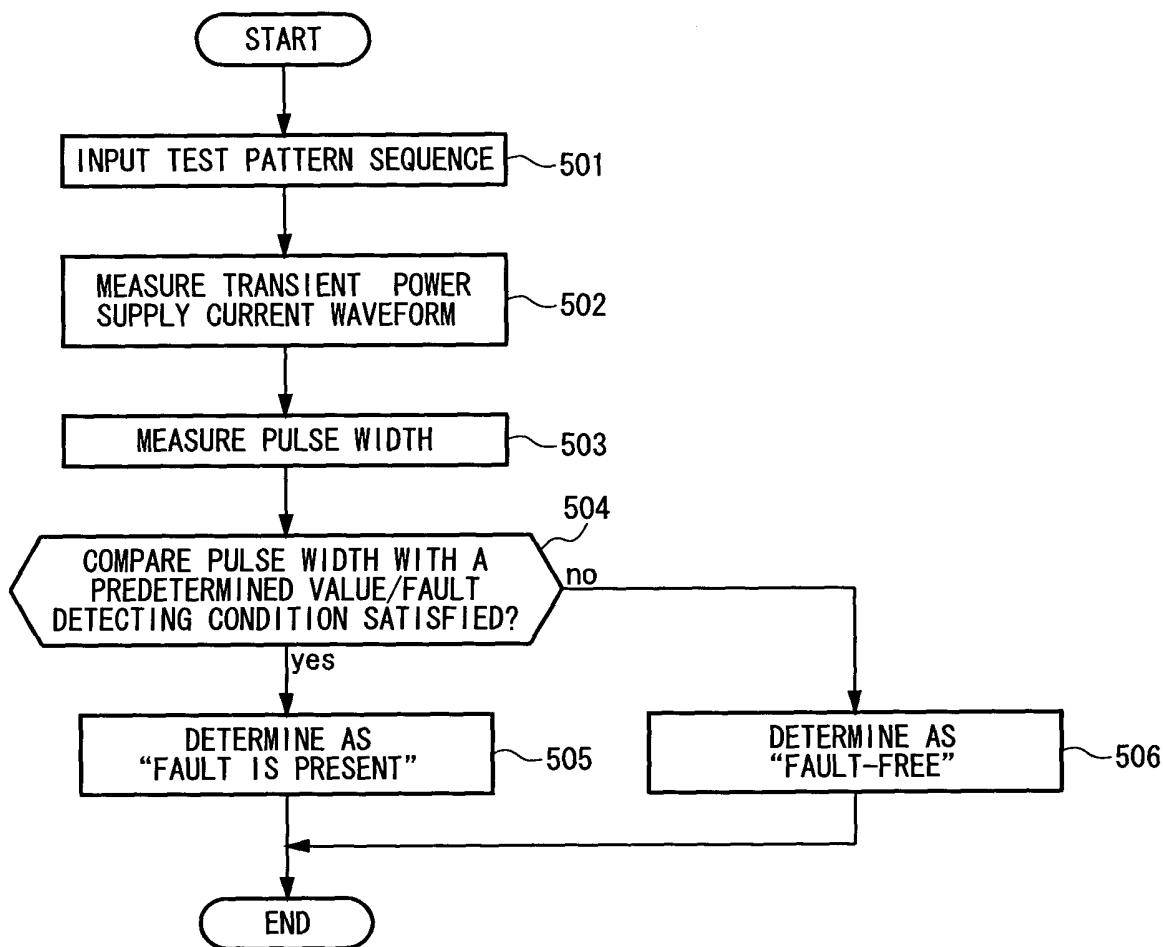


FIG. 24

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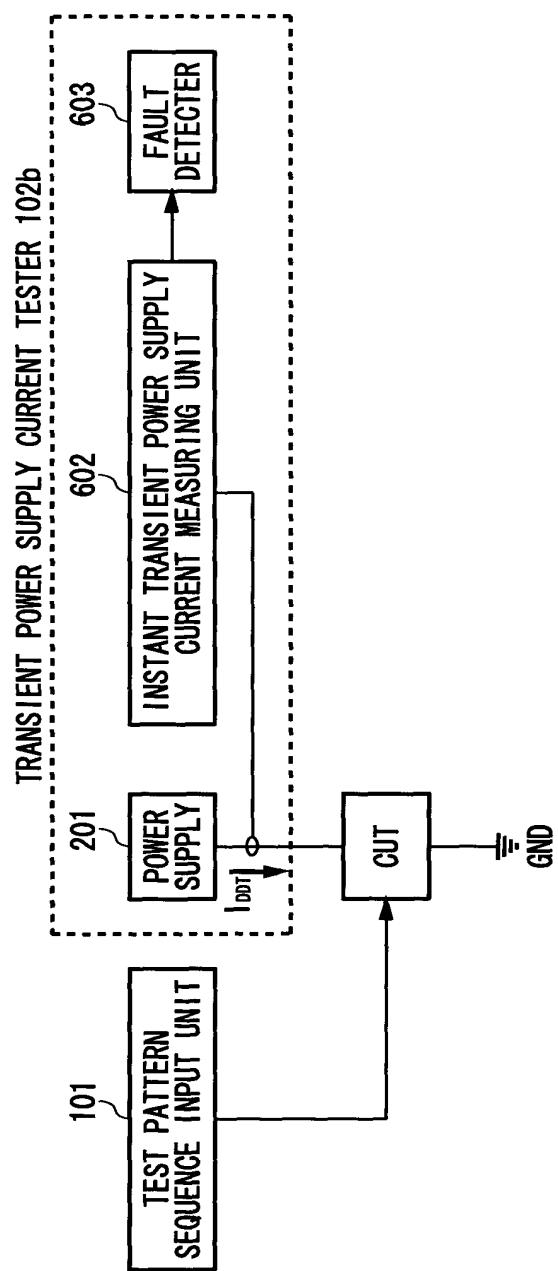


FIG. 25

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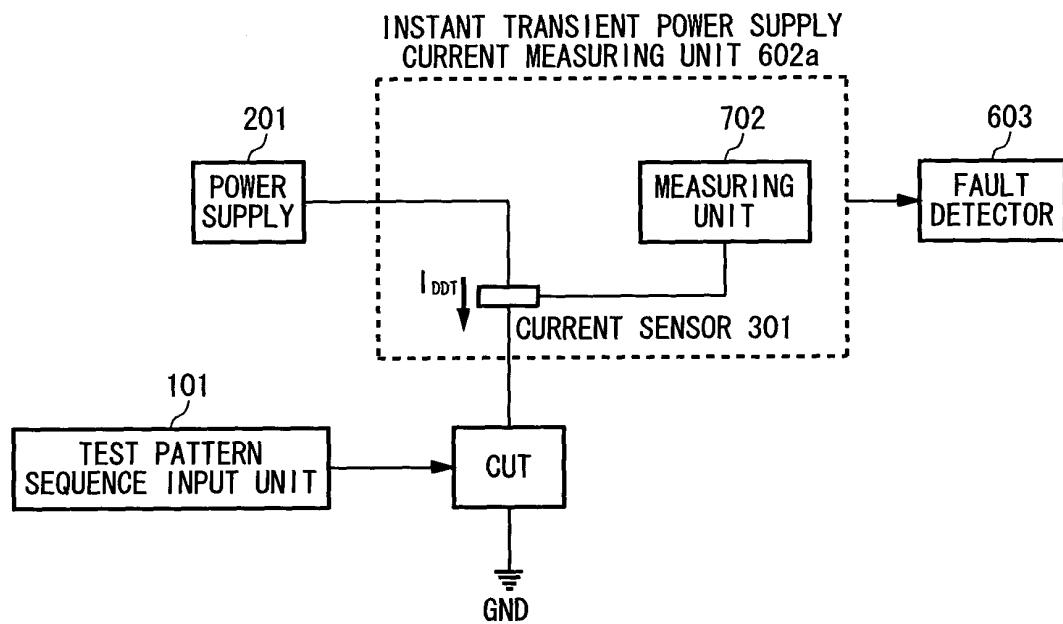


FIG. 26

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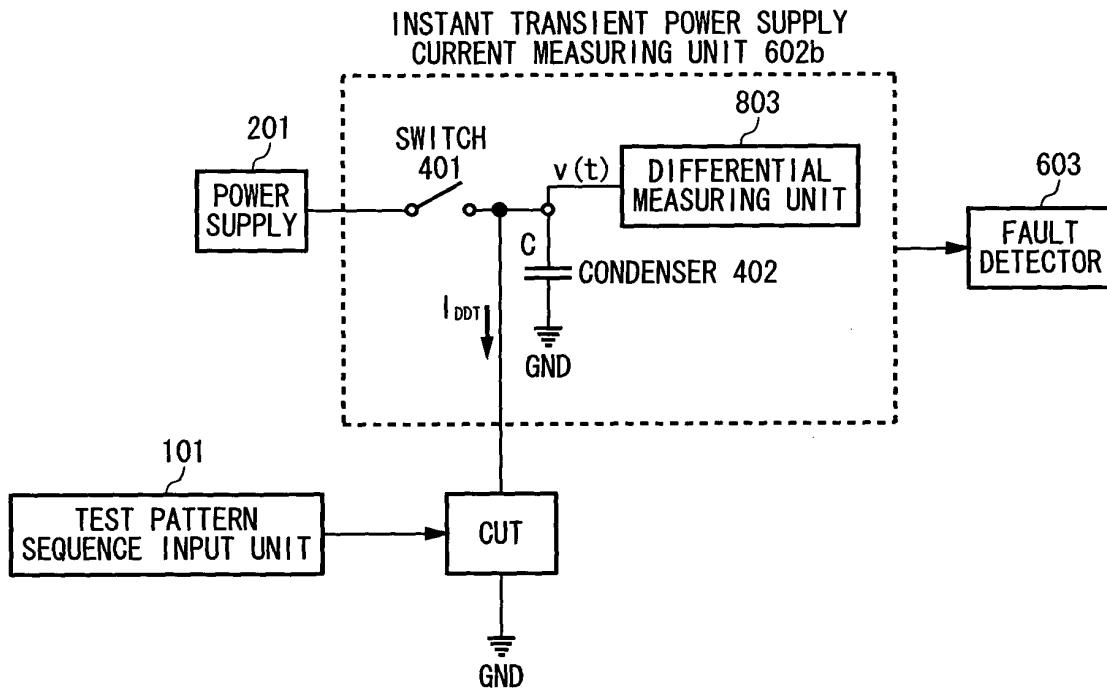


FIG. 27

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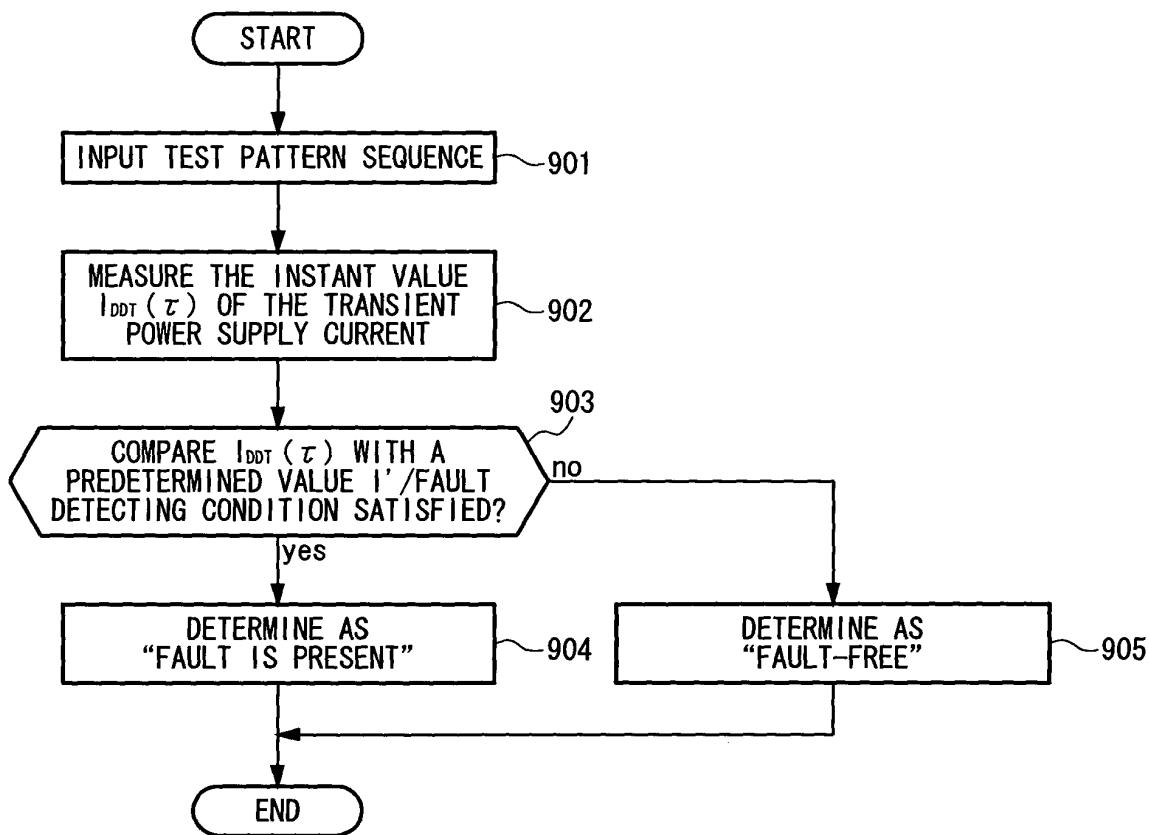


FIG. 28

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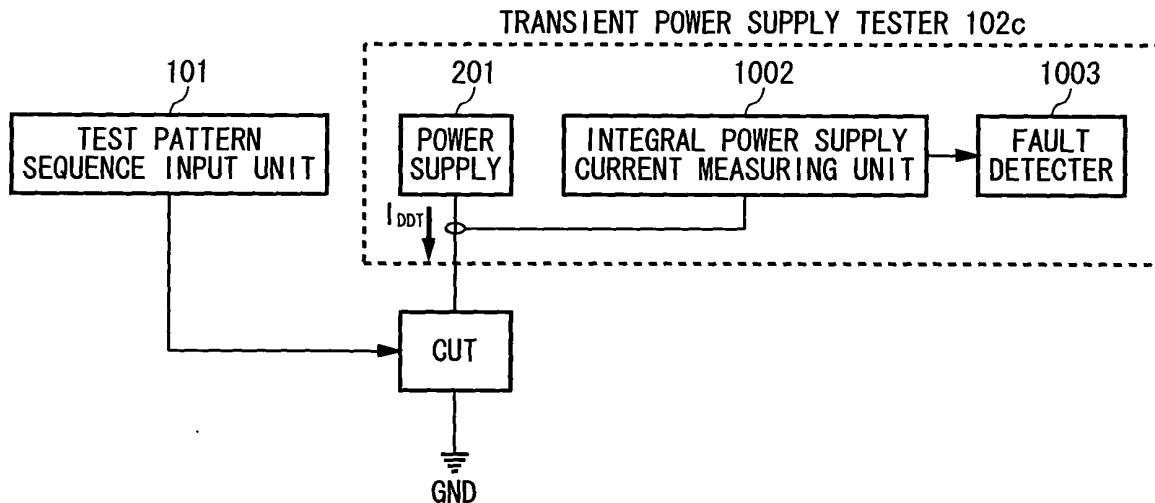


FIG. 29

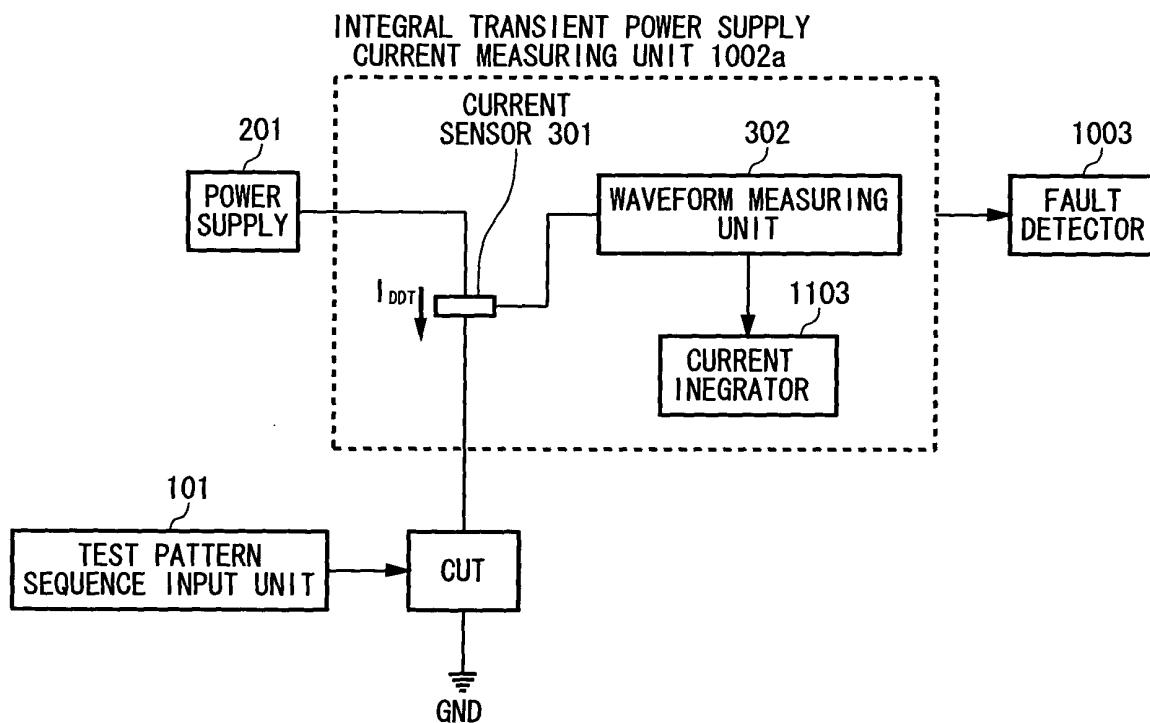


FIG. 30

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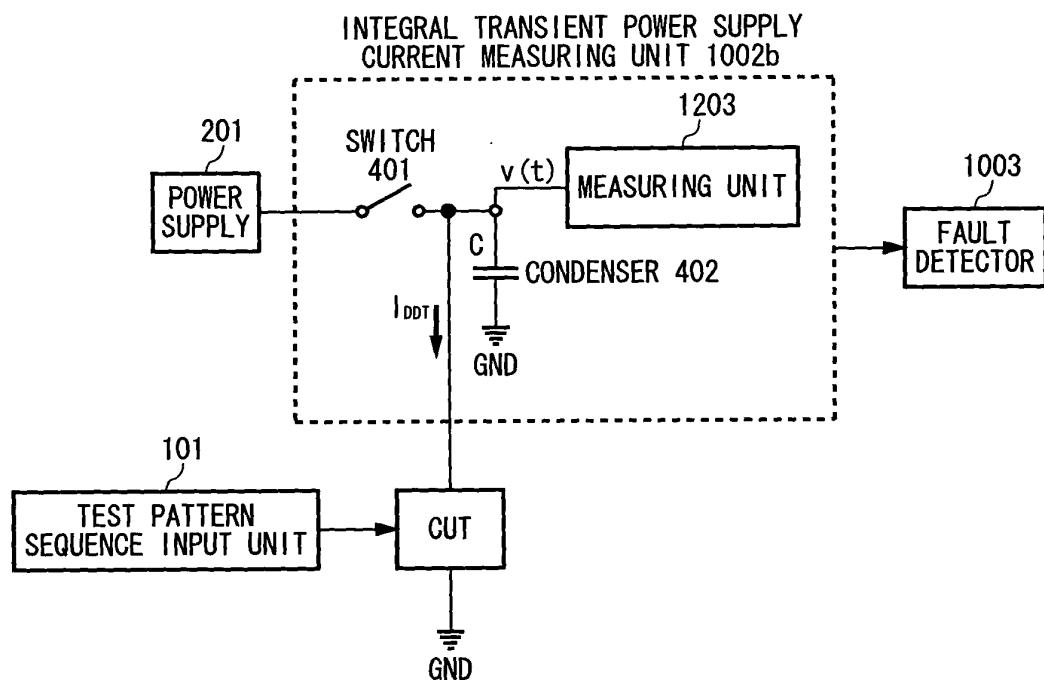


FIG. 31

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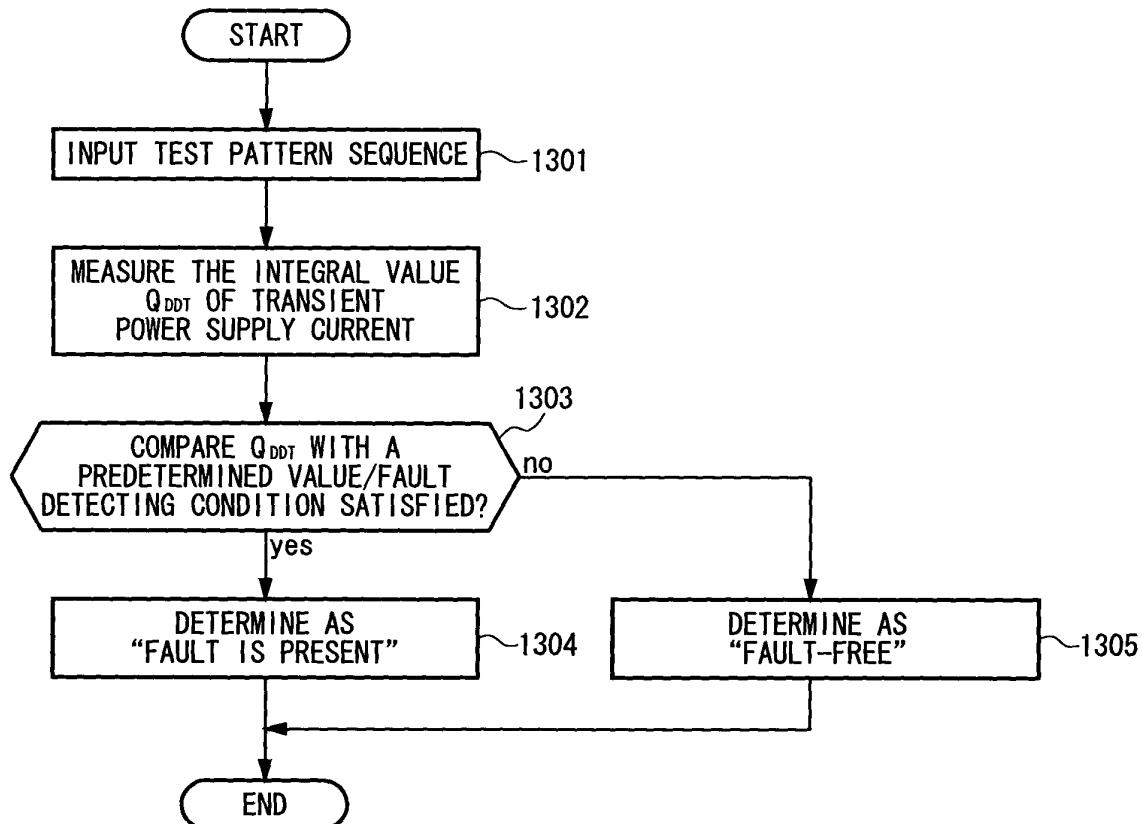


FIG. 32

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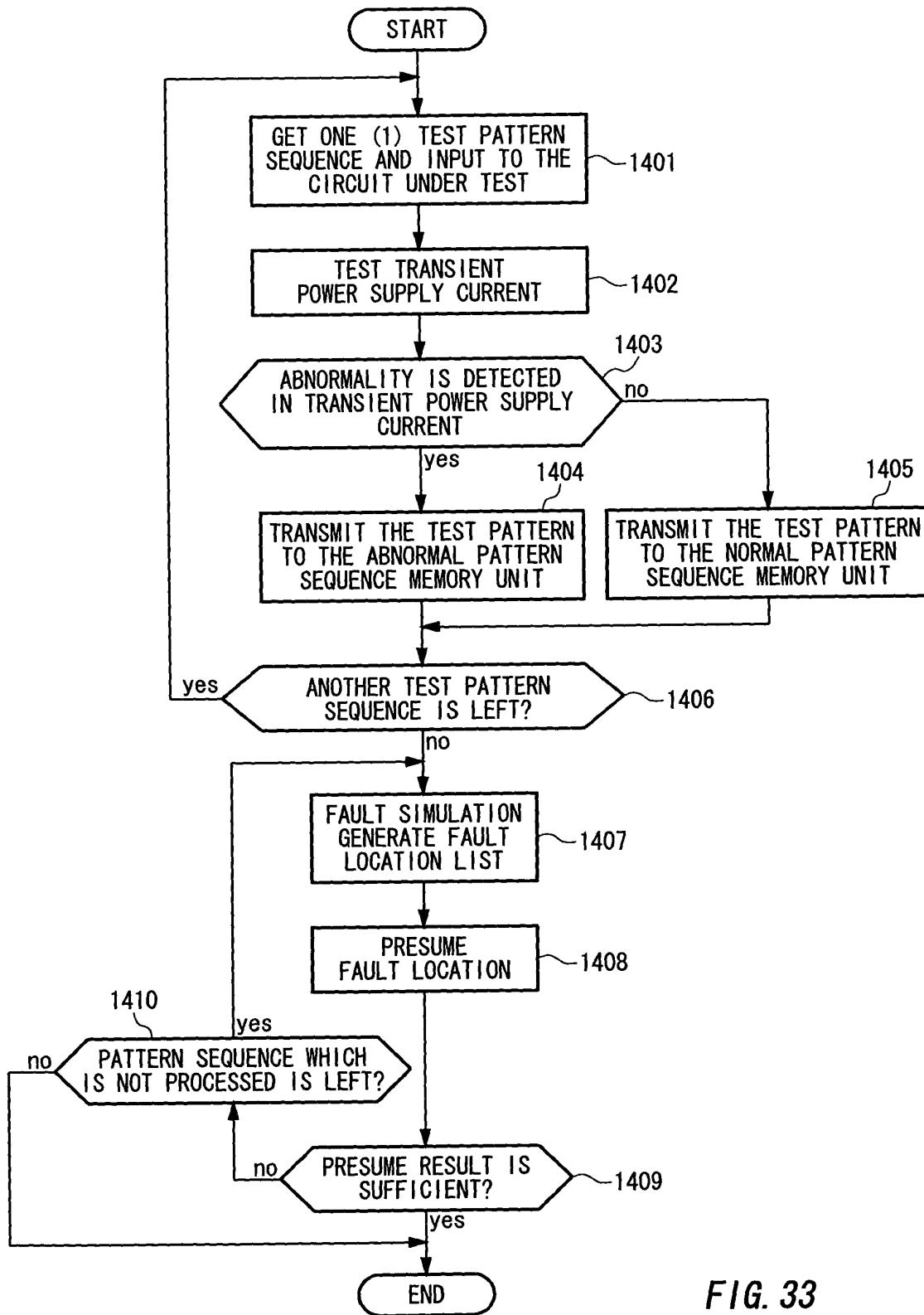


FIG. 33

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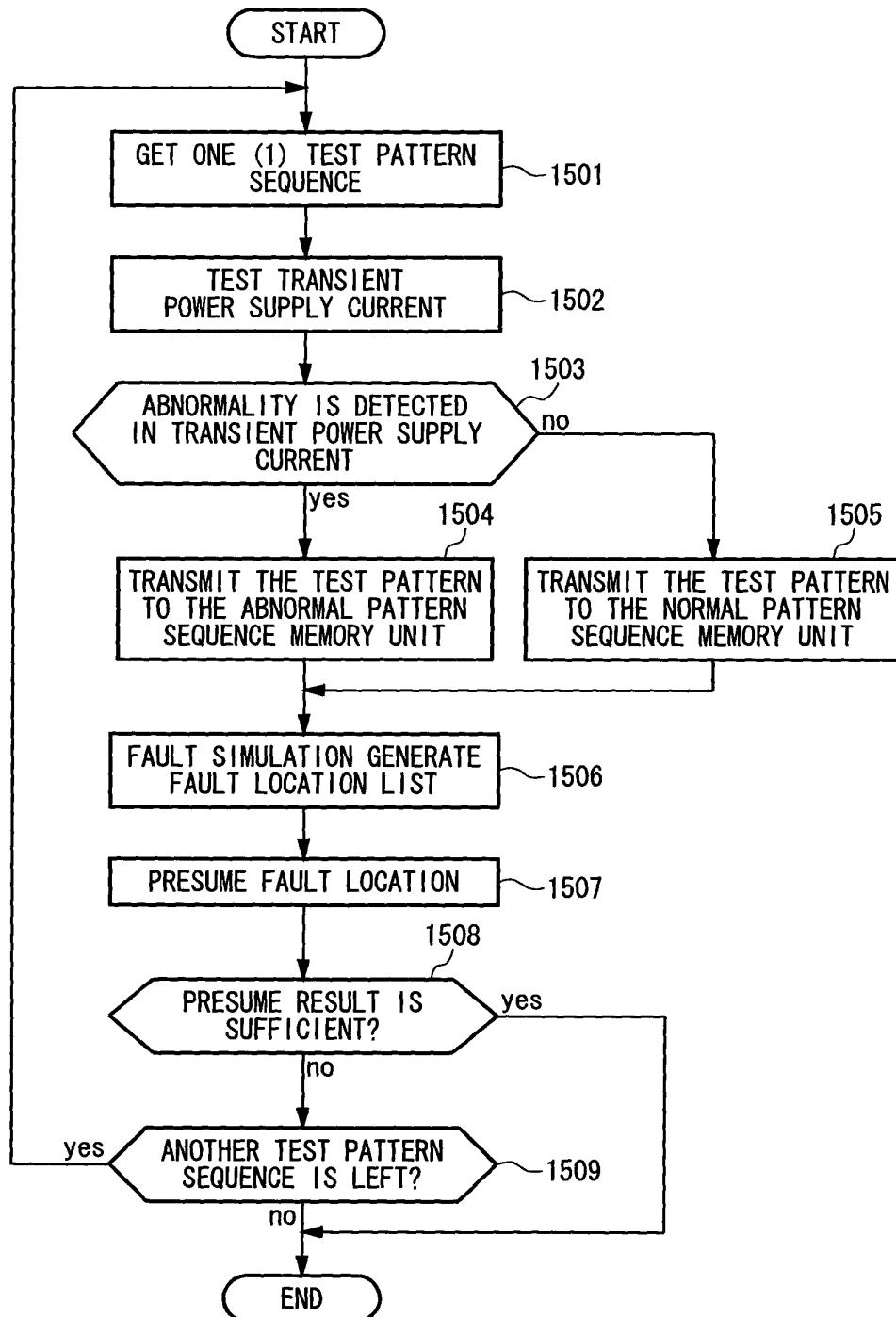


FIG. 34

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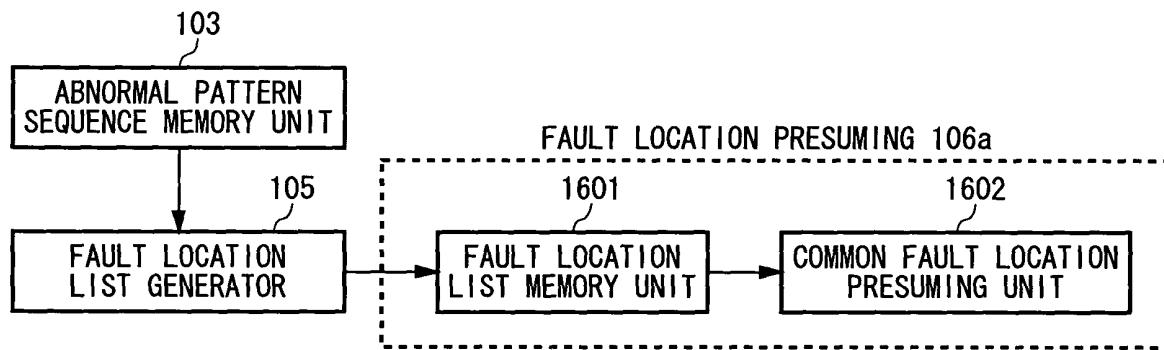


FIG. 35

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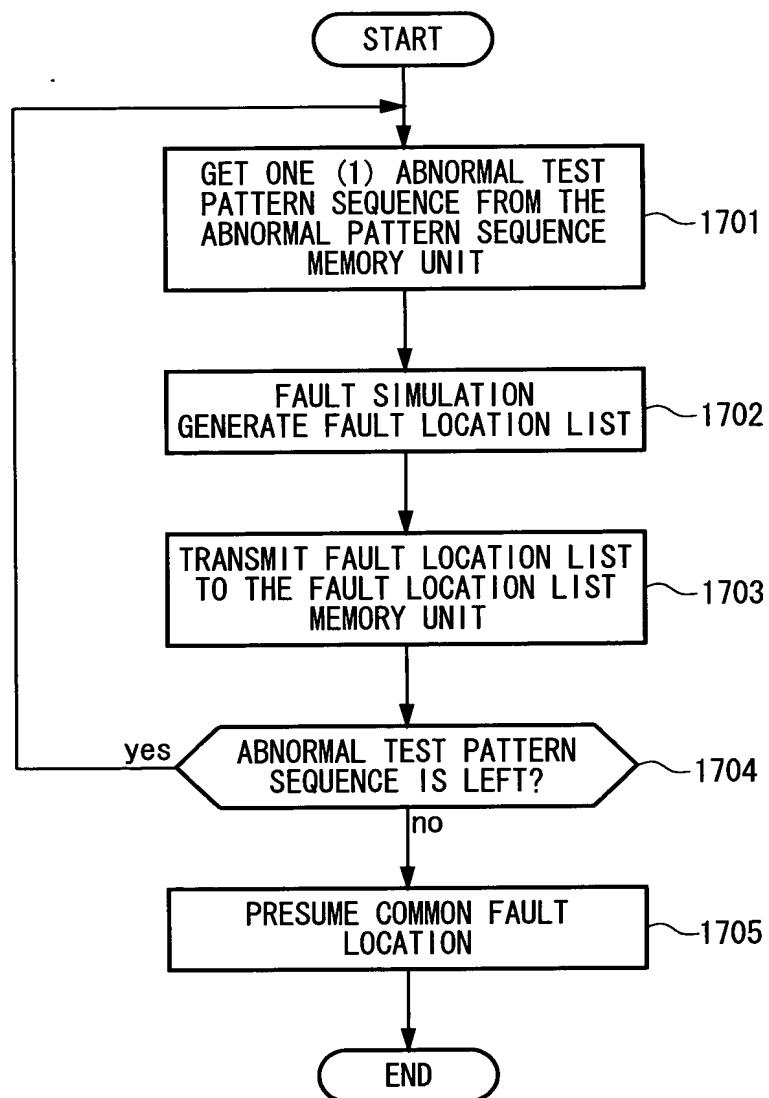


FIG. 36

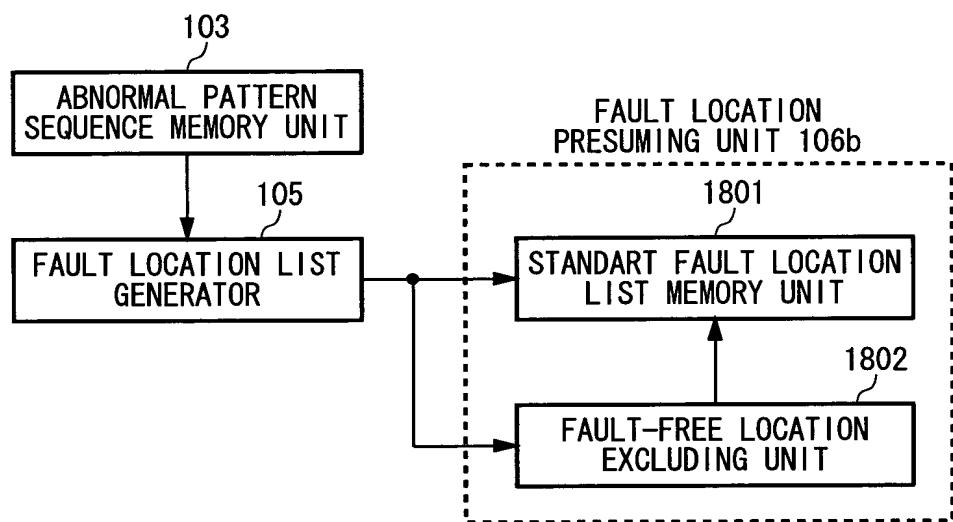


FIG. 37

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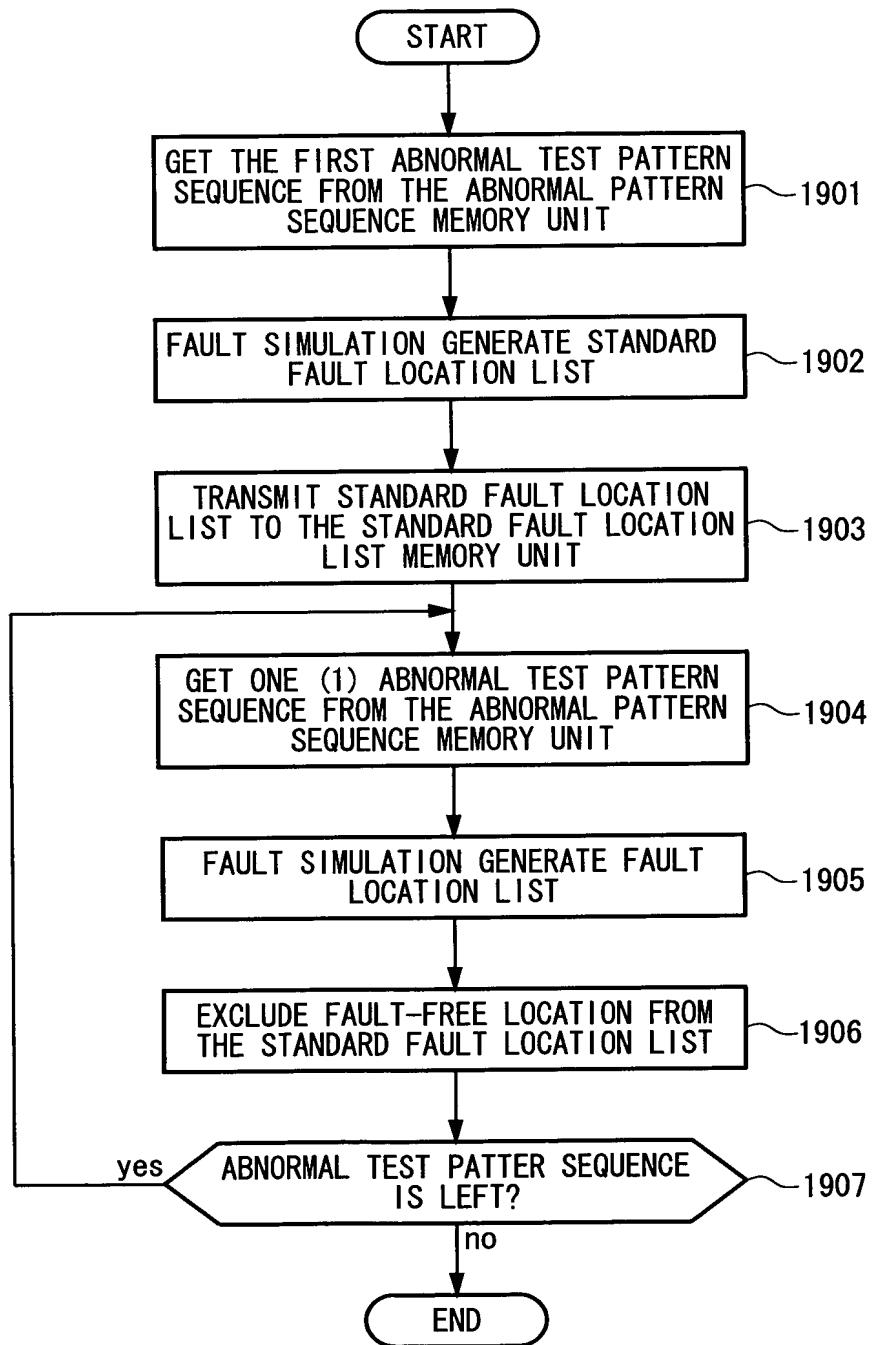


FIG. 38

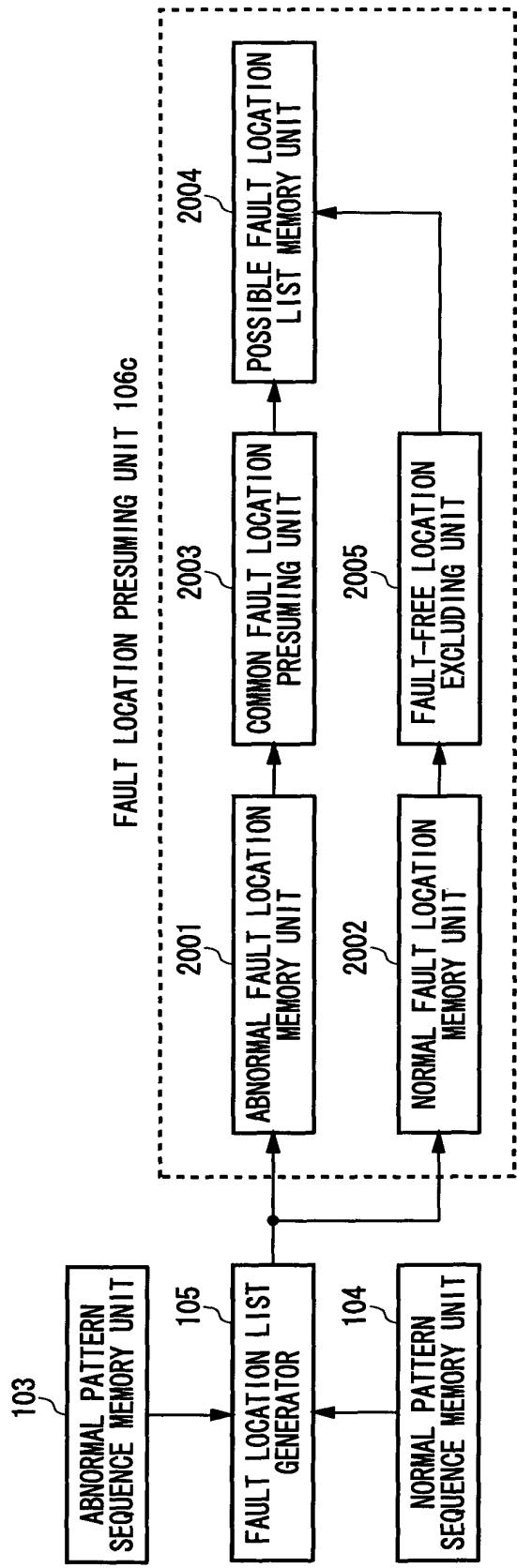


FIG. 39

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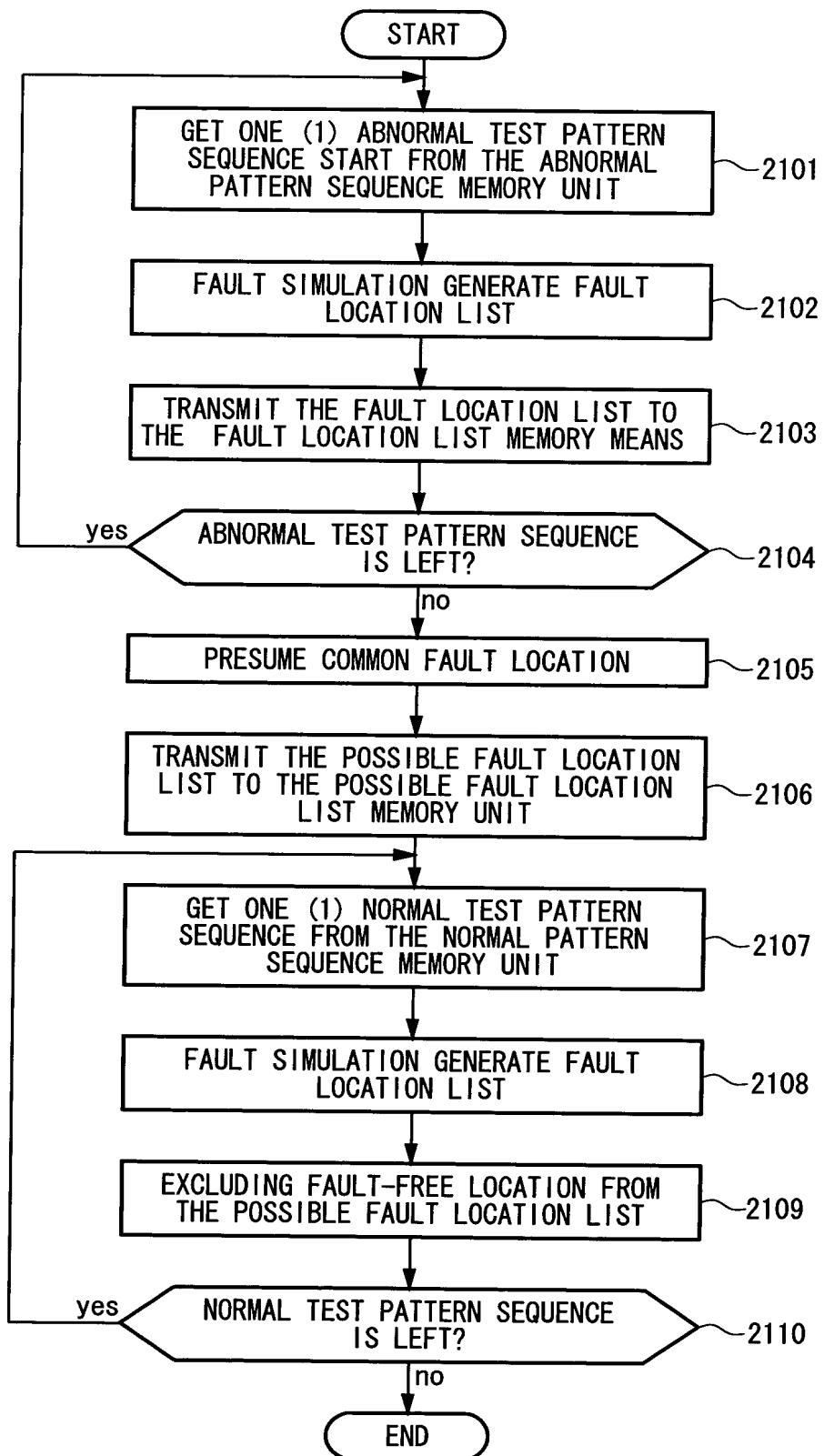


FIG. 40